--libraries

library ieee;

use ieee.std\_logic\_1164.all;

use ieee.std\_logic\_unsigned.all;

--entity------------------------------------------------------------------------------------------------------

entity lab2binaryadder is

port(

a : in std\_logic\_vector(7 downto 0);

KEY0, KEY1, SW9 : in std\_logic;

sum : out std\_logic\_vector(8 downto 0)

--carry : out std\_logic

);

end lab2binaryadder;

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--architecture------------------------------------------------------------------------------------------------

architecture a of lab2binaryadder is

signal sum\_temp, temp1, temp2 : std\_logic\_vector(8 downto 0);

begin

process(a, temp1, temp2, sum\_temp)

begin

if (SW9 = '0') then -- addition

if (KEY1 = '0') then --KEY1 assigns the first number to temp

temp1 <= ('0' & a);

end if;

if (KEY0 = '0') then

temp2 <= ('0' & a);

end if;

sum\_temp(8 downto 0) <= temp1 + temp2 ;

--carry <= sum\_temp(8);

sum <= sum\_temp(8 downto 0);

else --subtraction

if (KEY1 = '0') then --KEY0 assigns the first number to temp

temp1 <= ('0' & a);

end if;

if (KEY0 = '0') then

temp2 <= ('0' & a);

end if;

sum\_temp(8 downto 0) <= temp1 - temp2 ;

--carry <= sum\_temp(8);

sum <= sum\_temp(8 downto 0);

end if;

end process;

--elsif ( ) then

--subtractor code

--process( )

--begin

--sum\_temp <=

--end if;

end a;

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